MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : PE-EEE 601C VLSI And Micro Electronics

UPID : 006745

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following : [1 x 10 = 10]

(I) Give the different types of CMOS process?

(II) What are the various colour codes used in stick diagram?

(III) Write the syntax of procedure body?

(IV) What is the full form of FPGA?

(V) What is Enhancement mode MOSFET transistor?

(VI) What is meant by 'epitaxy'?

(VII) What are the various modelling used in Verilog?

(VIII) Write the major differences between PLA and PAL

(IX) What are the various regions of operation of MOSFET? How can we use these regions?

(X) What are the different MOS layers?

(XI) What are identifiers?

(XII) What is Latch – up?

Group-B (Short Answer Type Question)

Answer any three of the following : [5 x 3 = 15]

2. Classify the integrated circuits in terms of scale of integration. [5]
3. What are various types of scaling in MOSFET? Give examples. [5]
4. Draw the typical VLSI design flow-chart. [5]
5. Differentiate between strong and weak inversion of the channel of an E-MOS. [5]
6. Design Serial in Serial out shift register with suitable VHDL code. [5]

Group-C (Long Answer Type Question)

Answer any three of the following : [15 x 3 = 45]

7. (a) Describe the various features of VLSI design domains. [10]
   (b) Explain the term 'Regularity'. [5]
8. (a) List out the features of MOS-technology based IC design. [6]
   (b) Describe the basic structure of MOSFET and explain the difference for EMOS & DMOS. [7]
   (c) Define 'threshold voltage' of MOSFET. [2]
9. (a) Derive the expression of threshold voltage of the MOSFET. [6]
   (b) Explain the following in connection with the operation of an EMOS with relevant diagrams. [9]
   Accumulation, Depletion and Inversion.
10. (a) Draw the cross-section (profile) of a 4-terminal pMOS transistor and label all important regions of the device [4]
   .
   (b) Draw the top view of a 4-terminal pMOS transistor showing all of the layout layers and features necessary to construct a complete four-terminal device [4]
   .
   (c) A pMOS transistor has W = 1.5µm and L = 0.5µm. What is the oxide thickness of the gate capacitance, C_G, is 1fF ? Express your answer in angstroms. [3]
   (d) Explain CMOS inverter with relevant diagram. [4]
11. (a) Compare between Semi & Full custom design approach. [7]

(b) What do you mean by 'Standard cell-based design' ? [5]

(c) What is 'FPGA' ? [3]

*** END OF PAPER ***